IN THE CLAIMS

The listing of claims will replace all prior versions, and listing, of claims in the application:

Claim 1 (currently amended): An amplifier circuit, comprising:

an operational amplifier having a first input terminal, a second input terminal, and an output terminal;

a capacitive device coupled between the second input terminal and an input voltage; and

a resistor network comprising a plurality of stages connected serially, coupled between the second input terminal and the output terminal, wherein each stage of the resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and a common node; and

a second resistor coupled between the input node and the output node;

wherein an input and an output of the resistor network are the input node of the first stage and the output node of the last stage of the resistor network, respectively;

wherein a current of the input of the resistor network is larger than that of the output of the resistor network such that the amplifier circuit has a large-resistance capacitive time constant.

Claim 2 (previously presented): The amplifier circuit as claimed in claim 1, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 3 (previously presented): The amplifier circuit as claimed in claim 2, wherein the equivalent resistance of the resistor network is approximately 2n×R, wherein the resistor network includes n stages and the resistance of the second resistor is R.

Claim 4 (currently amended): An amplifier circuit, comprising:

an operational amplifier having a first input terminal, a second input terminal, and an output terminal;

a first resistor network comprising a plurality of stages connected serially, coupled to the second input terminal for receiving an input voltage, wherein each stage of the first resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and a common node; and

a second resistor coupled between the input node and the output node; and

a loading unit coupled between the second input terminal and the output terminal;

wherein the loading unit comprises a second resistor network;

wherein the second resistor network comprises a plurality of second stages connected serially;

wherein each second stage of the second resistor network comprises a second input node, a second output node, a third resistor coupled between the second input node and the common node, and a fourth resistor coupled between the second input node and the second output node.

Claim 5 (previously presented): The amplifier circuit as claimed in claim 4, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 6 (previously presented): The amplifier circuit as claimed in claim 5, wherein the equivalent resistance of the resistor network is approximately 2n×R, wherein the resistor network includes n stages and the resistance of the second resistor is R.

Claim 7 (canceled)

Claim ~~8~~ 7 (currently amended): The amplifier circuit as claimed in claim [[7]] 4, wherein the resistance of the third resistor is approximately two times larger than the resistance of the fourth resistor.

Claim ~~9~~ 8 (previously presented): The amplifier circuit as claimed in claim ~~8~~ 7, wherein the equivalent resistance of the second resistor network is approximately 2n×R, wherein the second resistor network includes n stages and the resistance of the fourth resistor is R.

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Claim ~~10~~ 9 (previously presented): The amplifier circuit as claimed in claim 4, wherein the loading unit comprises a capacitive device.

Claims 11-12 (canceled)

Claim ~~13~~ 10 (previously presented): The amplifier circuit as claimed in claim 4, further comprising a capacitive device coupled between the first resistor network and the input voltage.

Claim ~~14~~ 11 (previously presented): An amplifier circuit, comprising:

an operational amplifier having a first input terminal, a second input terminal, and an output terminal;

a capacitive device coupled between the second input terminal and the output terminal; and

a resistor network comprising a plurality of stages connected serially, coupled between the second input terminal and the output terminal, wherein each stage of the resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and a common node; and

a second resistor coupled between the input node and the output node;

wherein an input and an output of the resistor network are the input node of the first stage and the output node of the last stage of the resistor network, respectively;

wherein a current of the input of the resistor network is larger than that of the output of the resistor network such that the resistor network is operated as a large-resistance resistor.

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Claim ~~15~~ 12 (previously presented): The amplifier circuit as claimed in claim ~~14~~ 11, wherein the second input terminal is coupled to an input voltage.

Claim ~~16~~ 13 (previously presented): The amplifier circuit as claimed in claim ~~14~~ 11, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim ~~17~~ 14 (previously presented): The amplifier circuit as claimed in claim ~~16~~ 13, wherein the equivalent resistance of the resistor network is approximately 2n×R, wherein the resistor network includes n stages and the resistance of the second resistor is R.

Claim ~~18~~ 15 (previously presented): The amplifier circuit as claimed in claim ~~14~~ 11, further comprising a loading unit coupled between the second input terminal and an input voltage.